List of Claims:

Following is a complete listing of the claims pending in the application.

1-49. (Canceled)

50. (Original) A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate being coupled to the first microelectronic substrate to form a substrate assembly with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conformal conductive link coupled between the first and second connection sites, the conductive link conforming at least generally to a contour of the substrate assembly immediately adjacent to the conformal conductive link.

51. (Original) The package of claim 50 wherein the first and second connection sites face in at least approximately the same direction.

52. (Original) The package of claim 50 wherein the conductive link conforms to a plane at least approximately parallel to the first surface of at least one of the first and second microelectronic substrates.

53. (Original) The package of claim 50, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate; and

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material.

54. (Original) The package of claim 50, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

55. (Original) The package of claim 50 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

56. (Original) The package of claim 50, further comprising a dielectric material disposed on the first microelectronic substrate and wherein the conductive structure conforms to a contour of the dielectric material.

57. (Original) The package of claim 50 wherein the first microelectronic substrate has a first planform area in the plane of the second surface of the first microelectronic substrate and wherein the second microelectronic substrate has a second planform area in the plane of the second surface of the second microelectronic substrate, with the second planform area less than the first planform area.

58. (Original) The package of claim 50, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

59. (Original) The package of claim 50, further comprising an intermediate structure connected between the first and second microelectronic substrates.

60. (Original) The package of claim 50, further comprising an adhesive film disposed between the first and second microelectronic substrates.

61. (Original) The package of claim 50 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

62. (Original) The package of claim 50 wherein the conductive link is non-self-supporting.

63. (Original) The package of claim 50 wherein the first microelectronic substrate includes an SRAM device and the second microelectronic substrate includes a flash memory device.

64. (Original) The package of claim 50 wherein the conductive link is a first conductive link, and wherein the package further comprises:

a third microelectronic substrate coupled to the second microelectronic substrate, the third microelectronic substrate having a first surface with a third connection site, the third microelectronic substrate further having a second surface facing opposite the first surface, the second surface of the third microelectronic substrate facing toward the first surface of second microelectronic substrate; and

sequentially disposed first and second portions of a second conductive link disposed on the substrate assembly and extending between the third connection site of the third microelectronic substrate and the second connection site of the second microelectronic substrate.

65. (Original) A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate being coupled to the first microelectronic substrate with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conductive link coupled between the first and second microelectronic substrates, the conductive link including a first portion of a conductive material disposed on at least one of the first and second connection sites, the conductive link further including a second portion of a conductive material sequentially disposed on the first portion to link the first connection site to the second connection site.

66. (Original) The package of claim 65 wherein the conductive link conforms to at least one of the first microelectronic substrate and a dielectric material disposed on the first microelectronic substrate.

67. (Original) The package of claim 65 wherein the conductive link conforms to a plane at least approximately parallel to the first surface of at least one of the first and second microelectronic substrates.

68. (Original) The package of claim 65, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

69. (Original) The package of claim 65 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

70. (Original) The package of claim 65, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

71. (Original) The package of claim 65, further comprising an adhesive film disposed between the first and second microelectronic substrates.

72. (Original) The package of claim 65 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

73. (Original) The package of claim 65 wherein the conductive link is non-self-supporting.

74. (Original) A microelectronic device assembly, comprising:

a wafer having a plurality of non-singulated first microelectronic substrates, each first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a plurality of second microelectronic substrates each having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrates being coupled to the first microelectronic substrates while the first microelectronic substrates are non-singulated, and wherein the first surface of each first microelectronic substrate faces toward the second surface of a corresponding one of the plurality of second microelectronic substrates; and

a conductive link connected between the first and second connection sites.

75. (Original) The assembly of claim 74 wherein the conductive link conforms to a contour defined by the coupled first and second microelectronic substrates.

76. (Original) The assembly of claim 74 wherein the conductive link includes first and second sequentially deposited conductive portions.

77. (Original) The package of claim 74 wherein the first and second connection sites face in at least approximately the same direction.

78. (Original) The package of claim 74, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of the dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

79. (Original) The package of claim 74 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

80. (Original) The package of claim 74, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

81. (Original) The package of claim 74, further comprising an adhesive film disposed between the first and second microelectronic substrates.

82. (Original) The package of claim 74 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

83. (Original) The package of claim 74 wherein the conductive link is non-self-supporting.

84. (Original) A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the first microelectronic substrate being attached to the

second microelectronic substrate with the first surface of the first microelectronic substrate facing the second surface of the second microelectronic substrate and the first and second connection sites facing in at least approximately the same direction to define a microelectronic device assembly, wherein a planform area of the assembly in a plane generally parallel to the second surface of the first microelectronic substrate has a size and shape at least approximately identical to that of the second surface; and

a conductive link between the first and second connection sites.

85. (Original) The package of claim 84 wherein the conductive link conforms to at least one of the first surface of the first microelectronic substrate and a material disposed on the first surface of the microelectronic substrate.

86. (Original) The package of claim 84 wherein the first and second connection sites face in at least approximately the same direction.

87. (Original) The package of claim 84, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

88. (Original) The package of claim 84 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces, and wherein the package further comprises a microelectronic device external to the assembly and electrically coupled to the assembly while the edge is exposed.

89. (Original) The package of claim 84, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

90. (Original) The package of claim 84, further comprising an adhesive film disposed between the first and second microelectronic substrates.

91. (Original) The package of claim 84 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

92. (Original) The package of claim 84 wherein the conductive link is non-self-supporting.

93. (Original) An electronic device, comprising:

a housing; and

a microelectronic device package positioned within the housing, the microelectronic device package including:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic

substrate being coupled to the first microelectronic substrate to form a substrate assembly with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conformal conductive link coupled between the first and second connection sites, the conductive link conforming at least generally to a contour of the substrate assembly.

94. (Original) The device of claim 93 wherein the conductive link includes first and second portions of sequentially deposited conductive material.

95. (Original) The device of claim 93 wherein the packaged microelectronic device forms at least a part of a processor.

96. (Original) The device of claim 93 wherein the packaged microelectronic device forms at least a part of a memory.